

## DDR1/DDR2 SDRAM controller core

Product description 1.02

### Features

- Supports memory devices from major vendors
- Supports up to 4Gb DDR1/DDR2 devices
- Adheres to JEDEC standard
- Generic Application bus interface
- Supports multiple agents on application bus interface
- Supports multiple inbuilt arbitration schemes (RR, Weighted RR) or user defined arbitration schemes or external arbitration.
- Supports DDR1/DDR2 devices with 4 banks or 8 banks
- Supports buffered/non-buffered DIMMs
- Supports single/dual rank DIMMs
- Programmable CAS latency for DDR1/DDR2
- Programmable timing parameters viz.  $t_{RCD}$ ,  $t_{RP}$ ,  $t_{MRD}$ ,  $t_{RFC}$ ,  $t_{RRD}$ ,  $t_{CCD}$ ,  $t_{RDL}$ ,  $t_{RAS}$ ,  $t_{WF}$ , and  $t_{warhazard}$
- Fast page mode access
- Pipelined accesses inside controller
- Programmable auto-refresh time interval
- Configurable address mapping between application address bus and DDR row, column, bank addresses to suit to your applications bandwidth optimization
- Supports Power down and self refresh
- DLL based DDR data (DQ/DQS) interface
- On die termination support
- Manufacturer/Device dependant timing parameter file generation for register programming
- Available in Verilog/VHDL with extensive verification suite for functional, post-synthesis and post-layout verification
- Can be customized for the following:
  - Various Micro processors bus or specific application bus interface
  - Various speed grades
  - Various FPGA/ASIC vendors
  - For any user application

<b>DDR1/DDR2 SDRAM controller</b>	
<b>Core specifics</b>	
Library	TSMC-0.13u, LV-OD
Application Data width	128 bits
DDR Bus Data Width	64bits, 8 bits ECC
Total gate count	~50K (excluding PHY = ~5K gates)
Operating Frequency	333Mhz
Clock uncertainty	0.2ns
<b>Provided with Core</b>	
Documentation	Core Documentation
Design File Formats	Verilog/VHDL Source code Synthesis Scripts
Test Bench	Verilog Test Vectors
DDR-1/2 models for verification	Verilog models
Configuration file	Extracted from data sheet of DDR device to provide timing parameters for core
<b>Design Tool Requirements</b>	
Xilinx Core Tools	P&R tool
Entry/Verification Tools	Cadence, ModelTech
Synthesis Tools	Synopsys DC, Synplify Pro.
<b>Support</b>	
Support provided by Comit Systems, Inc.	

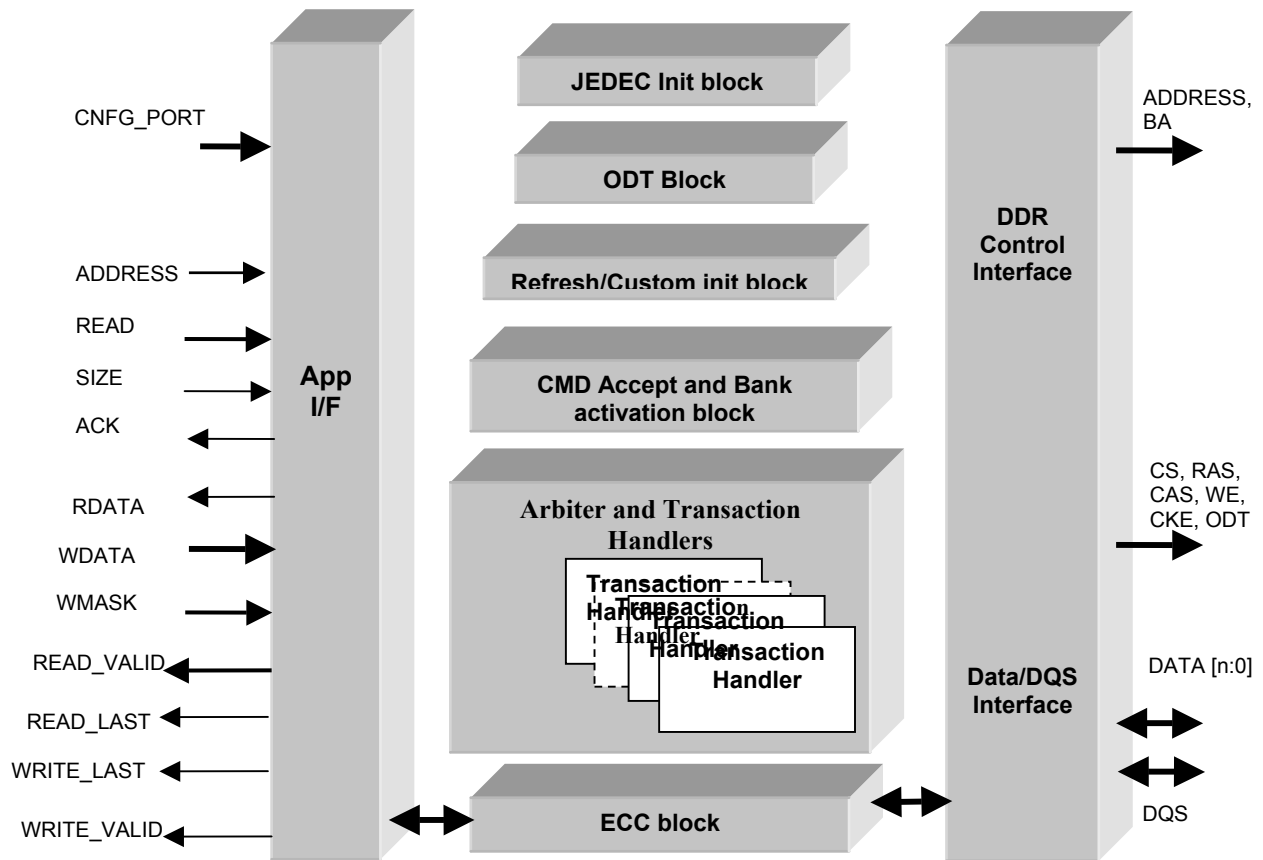


Figure 1. DDR SDRAM Controller Block Diagram

### General Description

This DDR2 controller can be used for interfacing with the DDR1 or DDR2 devices. All the timings  $t_{RCD}$ ,  $t_{RP}$ ,  $t_{MRD}$ ,  $t_{RFC}$ ,  $t_{RRD}$ ,  $t_{CCD}$ ,  $t_{RD_L}$ ,  $t_{RAS}$ ,  $t_{wr}$ , and  $t_{warhazard}$  are programmable for controller to be compatible with most of the devices from different vendors at the applications operating frequency. The address mapping between application bus address and Row/Column/Bank is configurable, so that the controller can be optimized for your application. The main blocks of controller are as follows:

- 1) Application Interface
- 2) JEDEC Initialization block
- 3) Refresh/Custom Initialization block
- 4) CMD Accept and Bank activation block
- 5) Transaction Handler and arbiter block
- 6) DDR Control combine block
- 7) Bank admin block
- 8) ODT Block
- 9) ECC Block

### Verification Methods

The DDR SDRAM Controller has been extensively tested using a test bench developed at Comit Systems Inc. The test bench is also available with the core.



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