COMIT® SYSTEMS
The Contract Engineering Company

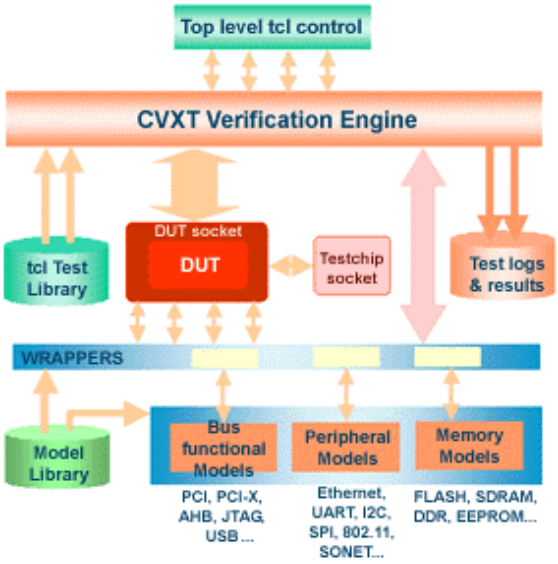
Fiesta® CVXT from Comit
Open Verification Environment

Fiesta® CVXT is a complete Open Verification Environment. It saves time by allowing rapid and painless implementation of module-interactive system level testing that is difficult to do in Verilog or C. Commonly available alternatives for system level verification require the designer to master an additional or proprietary syntax or language. In Fiesta® CVXT, tests are specified in Tcl using a set of just 12 commands. The CVXT Verification Engine provides the needed interactivity between tests and models to simulate a real-world environment.

Fiesta® CVXT offers the ability to build parallel, automated, synchronized self-checking verification testbenches for complex ASIC, SoC and programmable SoC designs. The environment bolts on to industry standard Verilog simulators and supports both real-world system testing and rigorous hardware module level and interface tests. The user can either run system level code intended for final silicon to test functionality, or do feature-by-feature self-checking of the chip modules, in parallel and in simultaneous interaction with other modules in the design.

Benefits

- Easy adoption due to open Tcl based environment
- Speeds up verification by automating real-world fully parallel testing
- Multiple test modes allows easy verification of design intent or rigorous checking of modules and interfaces
- Speedy testing of different prototypes provide rapid feedback for architecture adjustments
- Quickly tests different embedded processors by changing testchips and Bus Functional Models (BFM)
- Highly automated environment makes it convenient to run self-checking tests
- Completely scripted - requires no recompilation or elaboration, allowing for rapid changes



Key Features

- Sophisticated Verification Engine connects Verification Workbench to user-defined testbenches
  - Uses existing Verilog/C models
  - Supports industry standard Verilog simulators
  - Tests accuracy of modules and interfaces at the RTL level
  - Synchronizes tests with each other and with the simulator
  - Runs test in parallel and in simultaneous interaction with other modules in the design
  - Supports infinite number of parallel tests with independent execution contexts
  - Supports feature-by-feature self checking of modules
  - Supports if-then-else, events and triggers
  - Automatically waits for events and triggers from other interfaces

- Supports top-down test-my-chip or bottom-up check-all-modules-and-interfaces mode
- Supports execution of system level code to check functional intent
- Observes and logs results

- DUT Socket architecture enables easy testing of multiple prototypes
- Testchip Socket enables plugging in of embedded processor testchips
- Wrapper architecture supports integration of user defined and third party BFM and peripheral models from expandable model library
- Model library supports BFM and peripheral models

Specifications

Inputs

- DUT Verilog code
- BFMs, PMs and memory models: Verilog, C
- Tests: tcl
- Top level control: Tcl

Outputs

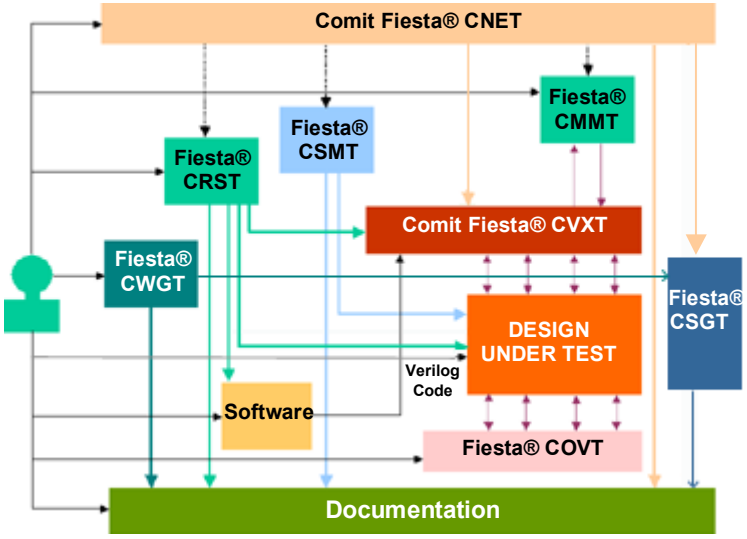
Test logs; Test results: .LOG, .RPT

Platforms

OS	Ver.	Simulator	Ver.
Solaris (Sparc)	2.7	nc-Verilog	3.2/3.3/3.4
Solaris (Sparc)	2.7	modelsim	5.6
Windows NT	4.0	nc-Verilog	3.4
Windows NT	4.0	modelsim	5.6

Comit Fiesta® CVXT is part of the Comit Fiesta® Process Standardization & Acceleration Toolkit. Individual tools are designed to work in standalone mode or in cascade, where the output of one tool can be used by another.

Fiesta® Process Standardization & Acceleration Toolkit is an integrated set of tools with a vision to painlessly transform specification to product, by producing as much of code and documentation automatically as possible, and simultaneously setting up a compatible verification environment from the start. Designers, therefore, are free to focus on designing state machines and creating tests. Coexists with industry standard EDA tools for simulation, synthesis and layout.



The toolkit consists of the following additional tools:

Fiesta® CRST Register Specification Tool
Accepts register bank definitions for a chip. Generates and regenerates documentation, software interface definitions, hardware implementations and verification definitions, preserving consistency, and avoiding errors

Fiesta® CSMT Finite State Machine Editor
Generates synthesizable Verilog code, and diagrams for documentation from state machines.

Fiesta® CMMT Simulation Memory Modeler
Generates dynamically configurable simulation time memory models that can be used in advanced system-level verification

Fiesta® CSGT Synthesis Script Generator
Accepts constrains and generates script to automate synthesis flow for popular synthesis tools

Fiesta® CAVT AHDL to VHDL Conversion tool
Converts Altera's proprietary HDL - AHDL to portable VHDL files to target any technology

Fiesta® CWGT Waveform Generation Tool
Produces output signal waveforms based on a GUI based input of signals and their transitions.

Fiesta® CNET Architectural Code Generation Tool
Accepts block level architectural input including third party IP and generates implementation roadmap by defining placeholders for all modules and interfaces

Fiesta® Process Standardization and Acceleration Tool Kit is an industrial strength suite of tools designed, developed, tested and used by engineers of Comit's Contract Engineering Center. Their experience in developing processes and methodology that yield predictable and accurate results forms the foundation of the toolkit. Use it with confidence.

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