**PCI TO PCI BRIDGE**

**Project Description 1.0**

**Features**

- Integration of Xilinx PCI Core
- 33MHz with full PCI 2.1 compliance
- Implemented in two Xilinx 4013E devices
- Interfaces two PCI buses on different devices
- Supports burst transfers
- Four Base Address registers
- Supports IO as well as memory operations.
- Includes functionality for keyboard, hard disk and other peripheral interfaces
- Protocol for inter bus communication
- Supports Programmable interrupt controller
- Silicon Proven

**Facts**

<table>
<thead>
<tr>
<th>PCI to PCI Bridge</th>
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<tbody>
<tr>
<td>Clock Speed</td>
<td>33 MHz</td>
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**Supported Devices**

<table>
<thead>
<tr>
<th>Device</th>
<th>CLBs</th>
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<tbody>
<tr>
<td>Xilinx</td>
<td>550 each</td>
</tr>
<tr>
<td>XC4013E-PQ240 (2 nos.)</td>
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**Design Tool Requirements**

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<th>Design Entry</th>
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<td>ViewSim</td>
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<td>Synthesis Tools</td>
<td>Synopsys Design Compiler</td>
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<td>Place and Route</td>
<td>XACT</td>
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Figure 1. System Level Block Diagram
General Description

The PCI to PCI bridge interfaced the PCI buses of two systems: a Mac and a Single-board PC. The Bridge allowed the Mac to read / write data from / to the PC, and vice-versa. The bridge logic included peripherals for the PC.

Functional Description

The design consisted of two PCI controllers one for the MAC side another for the PC side. The two controllers exchanged data over a proprietary bus. The MAC PCI controller contained both a master and target controller. The target controller enabled the MAC to read the internal registers and RAM of the controller as well as read the memory on the PC side. The master controller allowed the PC side to read/write memory on the MAC side.

The target on the PC PCI controller enabled the PC to read write the internal registers as well as to read/write MAC's memory. The master controller provided data from PC side when the MAC side requested.

The PCI controller on the MAC side also contained peripherals for the PC including keyboard controller, serial and parallel ports.

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